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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,937	06/24/2003	Nicholas A. Oleksinski	03-0228	1794

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LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,937	OLEKSINSKI ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/602937 filed on 06/24/03.

Claims 1-21 remain pending in the application.

Response to Arguments

Applicant's arguments with respect to claims 1-21 have been considered but are persuasive in view of the new ground's of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Rezek et al. Dennis (U.S Patent 5956256).

4. As to claims 1, Rezek et al. teach a method for generating a plurality of timing constraints for a circuit design, comprising the steps of: (A) identifying a plurality of clock signals by analyzing said circuit design (see fig 4a, 4b, 5a-5c col 10 lines 29 to col 12 lines 8); (B) determining a plurality of relationships among said clock signals (see fig 4a-4b, col 10 lines 28 to col 11 lines 26); and generating said timing constraints for said circuit design in response to said clock signals and said relationships (see fig 3, fig 7 and fig 9 and fig 10 col 9 lines 24 to col 10 lines 28 and col 12 lines 23-52 and col 15 lines 14-49).

5. As to claim 2, Rezek et al. teach wherein said plurality of clock signals comprises a test clock signal (see fig 4a-4b, col 10 lines 28 to col 11 lines 26).

6. As to claim 3, Rezek et al. teach further comprising the step of: eliminating from said timing constraints each signal connected to an internal mode pin for said circuit design that defines a non-clock signal (see fig 3 col 9 lines 24 to col 10 lines 28).

7. As to claim 4, Rezek et al. teach further comprising the step of: eliminating from said timing constraints each signal connected to an external interface for said circuit design that defines a non-clock signal (see fig 3 col 9 lines 24 to col 10 lines 28).

8. As to claim 5, Rezek et al. teach wherein step (C) is in further response to a plurality of parameters associated with said clock signals (see fig 4a-4b, and fig 5a-5c col 10 lines 28 to col 12 lines 8).

9. As to claim 6, Rezek et al. teach wherein at least one of said parameters relates to a test clock signals of said clock signals (see fig 4a-4b, and fig 5a-5c col 10 lines 28 to col 12 lines 8).

10. As to claim 7, Rezek et al. teach further comprising the step eliminating from said timing constraints each signal for said circuit design that defines a static signal (see fig 3 col 9 lines 24 to col 10 lines 28).

11. As to claim 8, Rezek et al. teach wherein step (B) comprises the sub-step of: generating an asynchronous relationship of said relationships between at least two of said clock signals operating asynchronously to each other (see fig 4a-4b and fig 5a-5c col 10 lines 28 to col 12 lines 8).

12. As to claim 9, Rezek et al.teach wherein step (B) comprises the sub-step of: generating a fastest clock relationship of said relationships between at least two of said clock signals operating at different speeds between two clock boundaries of said circuit design (see fig 4a-4b and fig 5a-5c col 10 lines 28 to col 12 lines 8).

13. As to claim 10, Rezek et al. teach wherein step (B) comprises the sub-step of: generating a multiplexed clock relationship of said relationships between at least two of said clock signals routable through a multiplexer in said circuit design (see fig 4a-4b and fig 5a-5c col 10 lines 28 to col 12 lines 8).

14. As to claim 11, Rezek et al. teach wherein step (B) comprises the sub-step of: generating a derivative clock relationship of said relationships between a first of said clock signals that is derived from a second of said clock signals (see fig 4a-4b and fig 5a-5c col 10 lines 28 to col 12 lines 8).

15. As to claim 12, Rezek et al. teach wherein step (B) comprises the sub-step of: generating a shared structure relationship of said relationships between a test clock signal of said clock signals and a normal clock signal particular structure of said circuit design in different modes for said circuit design (see fig 4a-4b and fig 5a-5c col 10 lines 28 to col 12 lines 8).

16. As to claim 13, Rezek et al. teach further comprising the step of: writing said timing constraints among a plurality of files (see fig 3, fig 7 and fig 9 and fig 10 col 9 lines 24 to col 10 lines 28 and col 12 lines 23-52 and col 15 lines 14-49).

17. As to claim 14, Rezek et al. teach a method for generating a plurality of timing constraints for a circuit design, comprising the steps of: identifying a plurality of clock signals by analyzing said circuit design (see fig 4a, 4b, 5a-5c col 10 lines 29 to col 12 lines 8); querying a user for a plurality of parameters said clock signals (see fig 4a-4b, col 10 lines 28 to col 11 lines 26); and generating said timing constraints response to said clock signals and said parameters (see fig 3, fig 7 and fig 9 and fig 10 col 9 lines 24 to col 10 lines 28 and col 12 lines 23-52 and col 15 lines 14-49).

18. As to claim 15, Rezek et al. teach further comprising determining a plurality of relationships among said clock signals, wherein said timing constraints are generated in further response said relationships.

19. As to claim 16, Rezek et al. teach wherein step (B) comprises the sub-step of: querying said user for a frequency parameter of said parameters f or each of said clock signals (see fig 4a-4b and fig 5a-5c col 10 lines 28 to col 12 lines 8).

20. As to claim 17, Rezek et al. teach wherein step (B) comprises the sub-step of: querying said user for a timing uncertainty parameter of said parameters for each of said clock signals (see fig 4a-4b and fig 5a-5c col 10 lines 28 to col 12 lines 8).

21. As to claim 18, Rezek et al. teach wherein said circuit design comprises a gate level design (see fig 2 col 8 lines 1 to col 9 lines 24).

22. As to claim 19, Rezek et al. teach wherein said circuit design comprises a register transfer language design (see fig 2 col 8 lines 1 to col 9 lines 24).

23. As to claim 20, Rezek et al. teach a storage medium comprising a medium and a computer program for use in a plurality of timing constraints recording said computer program the computer, said computer program including the steps (A) identifying a plurality of clock signals by analyzing said circuit design (see fig 4a, 4b, 5a-5c col 10 lines 29 to col 12 lines 8); a computer to generate for a circuit design, said medium that is readable and executable by (B) determining a plurality of relationships among said clock signals (see fig 4a-4b, col 10 lines 28 to col 11 lines 26); and (C) generating said timing constraints for said circuit design in response said clock signals and said relationships (see fig 3, fig 7 and fig 9 and fig 10 col 9 lines 24 to col 10 lines 28 and col 12 lines 23-52 and col 15 lines 14-49).

24. As to claim 21, Rezek et al. teach a storage medium comprising a medium and a computer program for use in a computer to generate a plurality of timing constraints for a circuit design, said medium recording said computer program that is readable and executable by the computer, said computer program including the steps of: identifying a plurality analyzing said circuit design (see fig 4a, 4b, 5a-5c col 10 lines 29 to col 12 lines 8); (B) querying a user for and a plurality of parameters for clock signals by said clock signals (see fig 4a-4b, col 10 lines 28 to col 11 lines 26); generating said timing constraints in response to said clock signals and said parameters (see fig 3, fig 7 and fig 9 and fig 10 col 9 lines 24 to col 10 lines 28 and col 12 lines 23-52 and col 15 lines 14-49).

Conclusion

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (571) 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-1908 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Binh Tat
Art unit 2825
August 18, 2005

THUAN DO
Primary examiner
8/18/05